AMENDMENTS TO THE CLAIMS

1. (currently amended) A circuit card comprising:

an integrated circuit having a plurality of inputs and a plurality of outputs;

a connector having a plurality of pins; and

a plurality of conductors, each of said plurality of conductors being coupled respectively between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said pins;

said plurality of ~~pins~~ conductors having a first portion for conducting bus signals and a second portion for providing a shield, said ~~pins~~ conductors in said first portion being grouped in a plurality of corresponding pairs, a respective one of said ~~pins~~ conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of ~~pins~~ conductors.

2. (original) The circuit card according to claim 1, wherein said shield is a ground shield.

3. (original) The circuit card according to claim 1, wherein said integrated circuit further comprises:

a driver to drive said signals between said inputs and said outputs of said integrated circuit.

4. (original) The circuit card according to claim 1, wherein said signals in each of said corresponding pairs are differential signals.

5. (original) The circuit card according to claim 1, wherein said integrated circuit is a memory device.

6. (currently amended) A circuit card comprising:

a connector having a plurality of pins;

a plurality of conductors, each of said plurality of conductors being coupled at a first end respectively to one of said plurality of pins; and

an integrated circuit having a plurality of inputs and a plurality of outputs, said conductors being coupled ~~between~~ at a second end respectively to one of said plurality of inputs ~~and one of said plurality of pins~~ or one of said plurality of outputs ~~and one of said plurality of pins~~;

said plurality of ~~pins~~ conductors having a first portion for conducting bus signals and a second portion for providing a shield, said ~~pins~~ conductors in said first portion being grouped in a plurality of corresponding pairs, a respective one of said ~~pins~~ conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of ~~pins~~ conductors.

7. (original) The circuit card according to claim 6, wherein said shield is a ground shield.

8. (currently amended) A circuit card comprising:

a first plurality of conductive traces connecting between contact pins and an integrated circuit to conduct signals, said first plurality of conductive traces being grouped in a plurality of corresponding pairs; and

a second plurality of conductive traces extending adjacent said first plurality of conductive traces to provide a shield, a respective one of said second plurality of conductive traces being located on each side of each of said plurality of corresponding pairs of said first plurality of conductive traces;

wherein said first plurality of conductive traces are part of a bus system.

9. (original) The circuit card according to claim 8, wherein said shield is a ground shield.

10. (original) The circuit card according to claim 8, wherein said signals in each of said corresponding pairs are differential signals.

11. (currently amended) A memory expansion card comprising:

a memory device having a plurality of inputs and outputs; ~~and~~

a connector having a plurality of pins; and

a plurality of traces, each of said plurality of inputs and ~~output~~ outputs of said memory device being coupled by a respective trace to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector, a first portion of said plurality of ~~pins~~ traces for conducting signals and a second portion of said plurality of ~~pins~~ traces for providing a shield, said ~~pins~~ traces in said first portion being grouped in a plurality of corresponding pairs, a respective one of said ~~pins~~ traces in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of ~~pins~~ traces;

wherein said first portion of said plurality of ~~pins~~ traces is part of a bus system.

12. (original) The memory expansion card according to claim 11, wherein said shield is a ground shield.

13. (original) The memory expansion card according to claim 11, wherein said signals in each of said corresponding pairs are differential signals.

14. (original) The memory expansion card according to claim 11, wherein said connector is adapted for connection to a motherboard.

15. (currently amended) A memory expansion card comprising:

a memory device having a plurality of inputs and a plurality of outputs;

a first plurality of conductive traces to conduct signals to said plurality of inputs or from said plurality of outputs, said first plurality of conductive traces being grouped in a plurality of corresponding pairs; and

a second plurality of conductive traces to provide a shield, a respective one of said second plurality of conductive traces being located ~~on~~ to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces;

wherein said first plurality of conductive traces are part of a bus system.

16. (original) The memory expansion card according to claim 15, wherein said shield is a ground shield.

17. (original) The memory expansion card according to claim 15, wherein said signals in each of said corresponding pairs are differential signals.

A1

18. (currently amended) A memory expansion card ~~connector~~ comprising:

a connector having a plurality of pins, said plurality of pins having a first portion for conducting signals and a second portion for providing a shield, said pins in said first portion being grouped in a plurality of corresponding pairs, a respective one of said pins in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of pins; and

a plurality of conductive traces connected respectively to each of said pins, a portion of said conductive traces being connected respectively to said pins in said second portion and extending respectively along each side of conductive traces connected to said first portion of pins,

wherein said first portion of pins is part of a bus system.

19. (currently amended) A processing system comprising:

a processing unit; and

a circuit card coupled to said processing unit, said circuit card comprising:

an integrated circuit having a plurality of inputs and a plurality of outputs;

a connector having a plurality of pins; and

a plurality of conductors, each of said plurality of conductors being coupled respectively between one of said plurality of inputs and one of said plurality of pins or one of said plurality of outputs and one of said plurality of pins;

said plurality of ~~pins~~ conductors having a first portion for conducting signals and a second portion for providing a shield, said ~~pins~~ conductors in said first portion being grouped in a plurality of corresponding pairs, a respective one of said ~~pins~~ conductors in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of ~~pins~~ conductors;

wherein said processing system comprises a bus system for passing signals through said processing system and said first portion of said plurality of pins are coupled to said bus system.

20. (original) The processing system according to claim 19, wherein said shield is a ground shield.

21. (original) The processing system according to claim 19, wherein each of said plurality of inputs and plurality of outputs of said integrated circuit are coupled to a plurality of pins of said connector.

22. (original) The processing system according to claim 19, wherein said integrated circuit further comprises:

a driver to drive said signals between said inputs and said outputs of said integrated circuit.

23. (original) The processing system according to claim 19, wherein said signals in each of said corresponding pairs are differential signals.

24. (original) The processing system according to claim 19, wherein said integrated circuit is a memory device.

25. (original) The processing system according to claim 19, wherein said processing unit and said integrated circuit are on a same chip.

26. (currently amended) A processing system comprising:

a processing unit; and

a memory expansion card coupled to said processing unit, said memory expansion card comprising:

a memory device having a plurality of inputs and a plurality of outputs; ~~and~~

a connector having a plurality of pins; and

a plurality of traces, each of said plurality of inputs and said plurality of outputs of said memory device being coupled by a respective trace to at least one of said plurality of pins to receive signals from or send signals to said pins of said connector, a first portion of said plurality of ~~pins~~ traces for conducting signals and a second portion of said plurality of ~~pins~~ traces for providing a shield, said ~~pins~~ traces in said first portion being grouped in a plurality of corresponding pairs, a respective one of said ~~pins~~ traces in said second portion being located on each side of each of said plurality of corresponding pairs of said first portion of said plurality of ~~pins~~ traces;

wherein said processing system comprises a bus system for passing signals through said processing system and wherein said first portion of said plurality of pins are coupled to said bus system.

27. (original) The processing system according to claim 26, wherein said shield is a ground shield.

28. (original) The processing system according to claim 26, wherein said signals in each of said corresponding pairs are differential signals.

29. (original) The processing system according to claim 26, further comprising:

a motherboard, wherein said connector is adapted for connection to said motherboard.

30. (currently amended) A processing system comprising:

a processing unit; and

a memory expansion card coupled to said processing unit, said memory expansion card comprising:

a memory device having a plurality of inputs and a plurality of outputs;

a first plurality of conductive traces to conduct signals to said plurality of inputs or from said plurality of outputs, said first plurality of conductive traces being grouped in a plurality of corresponding pairs; and

a second plurality of conductive traces to provide a shield, a respective one of said second plurality of conductive traces being located ~~on~~ to extend along each side of each of said plurality of corresponding pairs of said first plurality of conductive traces;

wherein said first plurality of conductive traces are part of a bus system of said processing system.

31. (original) The processing system according to claim 30, wherein said shield is a ground shield.

32. (original) The processing system according to claim 30, wherein said signals in each of said corresponding pairs are differential signals.

33. (currently amended) A method for constructing a circuit card for a bus system comprising the steps of:

providing a first plurality of pins on a connector of said circuit card, said first plurality of pins for conducting bus signals;

grouping said first plurality of pins into a plurality of corresponding pairs; and

providing a second plurality of pins on said connector of said circuit card, said second plurality of pins being connected to a respective conductive trace extending along each side of pairs of traces connected to each corresponding pair of said first plurality of pins for providing a signal shield~~; and~~

~~locating a pin of said second plurality of pins adjacent to each side of said corresponding pairs of pins of said first plurality of pins~~.

34. (original) The method according to claim 33, further comprising:

coupling each of said second plurality of pins to a ground potential.

35. (original) The method according to claim 33, wherein said step of grouping said first plurality of pins further comprises:

grouping said first plurality of pins into a plurality of corresponding pairs, wherein said pins in each corresponding pair are adapted to conduct differential signals.